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The Soft Core Processors: A Review

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Abstract: Embedded systems are characterized by small size, high speed and minimum power requirements. Apart from satisfying these characteristics, the embedded products need to meet some design metrics viz. time to prototype, time to market, Non Recurring Engineering (NRE) Cost. So as to meet some of these requirements and to speed up the process of hardware-software co-design, soft CPU cores are made available by different manufacturers. This has simplified the job of an embedded product designer to a great extent. Soft-core processors play a vital role due to their ease of usage. Soft-core processors have advantages like reduced cost, flexibility, platform independence and greater immunity to obsolescence over their hard-core counterparts. The soft CPUs come with different features. Some soft CPUs are open source while others are proprietary; some are of RISC category while others are of CISC type. Based on product development requirements, an appropriate soft CPU core could be selected. This paper presents review on features of a few soft core processors, which are popular in the embedded development market.

Keywords: Time to Prototype, Time to market, NRE Cost, open- source, soft-core processors, RISC, CISC.

I. INTRODUCTION

Field Programmable Gate Array (FPGA) devices are used normally for implementation of parallel algorithms while microprocessors are well known for sequential algorithms. Application Specific Integrated Circuit (ASIC) design sometimes need combination of both pertaining to constraints like minimum power consumption, small area and fewer problems with signal integrity and EMI (Electromagnetic interference). New industry requirements diminish the life-cycle of microcontrollers, and several processors became obsolete in shorter periods of time. The biggest challenge to Hardware architects is fulfillment of new requirements; which are adaptable characteristics, high performance and power efficiency and reduction in time to design the product. Flexibility and adaptability are considered synonyms of reconfigurable technologies. For fast development of System-on-Programmable-Chip (SoPC), many commercial processors offer memory and logic elements with a large variety of intellectual Property (IP) peripherals. Also, reconfigurable systems on a chip became a reality with soft- core processor [1]. The available Electronic-Design-Automation (EDA) tools help us in constructing prototypes of Systems-on-a- Chip rapidly and in a very mature way [2]. Hardware Description Language (HDL) is used for such prototyping.

The paper is organized in four sections as below: Section II summarizes advantages of using soft-core processors. In section III, a review of several soft-core processors from major commercial vendors as well as open-source communities is covered. We conclude in section4with few comments on future work in the area of soft-core processors as well as a comparison among major soft core processors based on important features such as clock frequency, word-length, pipeline stages etc.

II. SOFT CORE PROCESSORS: A SOLUTION FOR RAPID PROTOTYPING

A soft-core processor is one that is implemented entirely in the logic primitives of an FPGA using VHDL. The soft-core processor does not have the speeds or performance characteristics of a hard-core or a discrete processor. In many embedded applications, high performance is not of prime concern compared with required functionality and flexibility.

A soft-core processor allows a designer to add or subtract peripherals from the SoPC with ease. A soft-core processor also offers the flexibility of configuring the core itself for the application. Using a SoPC solution also offers flexibility outside the FPGA while designing the circuit board. A discrete microprocessor solution has a fixed pinout, sometimes making routing difficult. Since a SoPC exists in an FPGA, the pinout is flexible, which gives the board designer almost complete freedom with component placement while meeting the timing constraints [3].

Another benefit is that there are more General Purpose I/O pins (GPIO) available in a SoPC solution compared to a discrete microprocessor. Using a soft-core processing solution can reduce schedule in both, design and verification phases of a project.

Characteristics of popular soft core processors viz. word length; category and processing speed are considered for comparison amongst the soft core processors in following section.

III. A SURVEY OF SOFT CORE PROCESSORS

The following section covers a survey of major soft core processors available from major commercial vendors as well as open-source communities.

A. OpenSPARC T1

The complete multiprocessor chip implementation from Sun Microsystems is shown in Fig. 1. It has 64-bit SPARC V9 architecture and targeted towards commercial applications such as application servers and database servers. It contains eight SPARC processor cores. Each SPARC core has an instruction cache, a data cache, and a fully associative instruction and data translation look-aside

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buffers (TLB). The eight SPARC cores are connected through a crossbar to an on-chip unified level 2 cache (L2-cache). There is an on-chip J-Bus controller to provide interconnect between the OpenSPARC T1 processor and I/O subsystem.

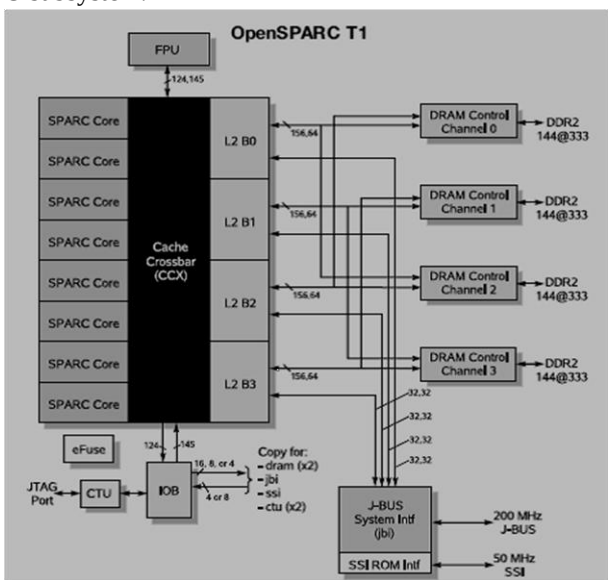

Fig. 1: OpenSPARC T1 Processor [4].

Features of OpenSPARC T1 processor include 16 KB L1 Instructions Cache per CPU, 8 KB L1 Data Cache per CPU, 3 MB L2 Cache shared by all CPU's, and an IEEE 754 compliant FPU shared by all CPU's [4].

B. RISC S1 Core

Simply RISC S1 Core is a cut down version of the OpenSPARC processor released as open-source by Sun Microsystems.

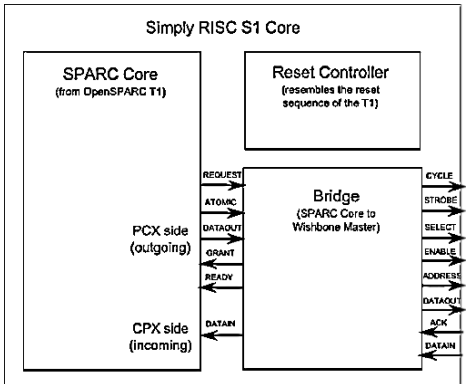

Fig. 2: Simply RISC S1 Core [7].

The block diagram of Simply RISC S1 core is shown in fig. 2. Simply RISC S1 Core has a 64-bit SPARC Core with a Wishbone/AMBA bridge, an interrupt controller and a simple reset controller [7]. It follows the SPARC v9 64-bit ISA, and has 64-bit wide Data Bus and Address Bus. S1 core has a 6-stage integer pipeline.

C. OpenRISC1200 (OR1200)

The OpenRISC 1200 (OR2100) is a synthesizable CPU core maintained by the developers at OpenCores.org. The block diagram of OpenRISC1200 developed by OpenCores is shown in Fig. 3.This is an open source implementation of the OpenRISC 1000 architecture in Verilog RTL. The OR1200 is a 32-bit scalar RISC with Harvard micro architecture [5]. The main features of OR1200 include a 5-stage integer pipeline, virtual memory support (MMU) and basic DSP capabilities. It has 32 bit instructions and can operate on 32-bit or 64-bit data. Default Data and instruction cache are 1-way direct-mapped 8KB with 16-byte line size each.

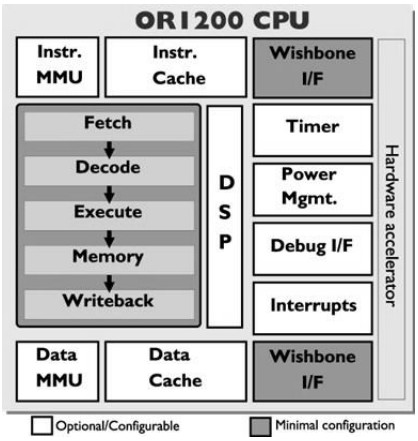

Fig. 3: OR1200 System [5].

Both caches are physically tagged. MMUs have data and instructions TLB's both. Each TLB is 64-entry hash based one way direct-mapped. It is amongst one of the high performing soft-core processors with 300 Dhrystone [6] 2.1 MIPS at 300 MHz using 0.18uprocess. It supports very few FPGA development boards and its debugging solutions are complicated.

D. Nios II

The Nios II is a proprietary 32-bit RISC architecture processor core from Altera for use in their FPGAs. Block diagram of NIOS II Processor is shown in fig. 4. NIOS II has load-store RISC architecture. The system designer can define a custom Nios II core based on application requirements. The reconfiguration can be at the level of data path width (16 bit or 32 bit) or register file size or cache size or even at defining custom instructions to be used. Even a predefined memory management unit (MMU) can be added to the basic Nios II to extend its functionalities.

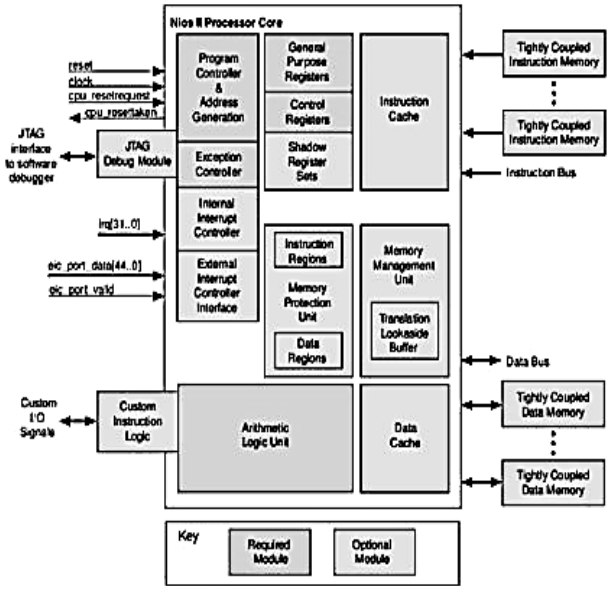

Fig. 4: Nios II Processor Core Block Diagram [8].

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NIOS II/*f* has 6-stage pipeline and executes one instruction per cycle. It has separate Instruction and Data cache. The Nios II Integrated Development Environment (IDE) is available for building, running, and debugging software of several platforms. The main features of Nios II include Easy-to-use IDE's and no need of using an extra JTAG programming tool. Altera Quartus II and Nios II Embedded Design Suite helps user to build a NIOS II-based system and to write system specific application software. The main problem is Nios II can only be used in Altera FPGAs [8].

E. MicroBlaze

This is a proprietary 32-bits RISC reconfigurable soft-processor from Xilinx, and can be customized with different peripheral and memory configurations.

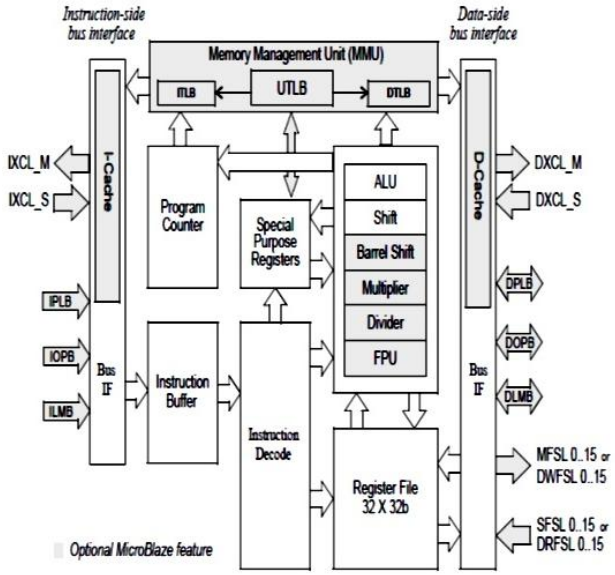

Fig. 5: Xilinx MicroBlaze core block diagram [9].

Harvard memory architecture is used for development of MicroBlaze and was first released in the year 2001. Still new functions are being added on to the basic MicroBlaze architecture [2]. Fig.5 shows block diagram of Xilinx MicroBlaze core. This processor has a three-stage pipeline with variable length instruction latencies, typically ranging from one to three cycles. Xilinx Platform Studio is available for creating a MicroBlaze based system. It uses 2 Local Memory Busses (LMB) to connect instruction and data memories. User can define the sizes of instruction and data memory and the number of peripheral based on application requirements. An On-Chip-Peripheral Bus (OPB) is used to boost systems performance and it is designed to support low- performance/speed peripherals such as UART, GPIO, USB, external bus controllers [9]. This soft-core processor be used only in Xilinx FPGAs only and has lots of configuration options. It also uses the Advanced Extensible Interface (AXI) standard bus. Being proprietary soft-core, the source code is not available.

F. The SecretBlaze

The SecretBlaze, shown in Fig. 6, is developed using VHDL. This is a 32-bit RISC processor compliant with the instruction set of MicroBlaze. Its internal architecture is mainly based on DLX processor [16].

The main features of this soft CPU include a 5-stage pipeline and 32-bit addresses providing a 4 GB linear address space with 32-bit word-length.

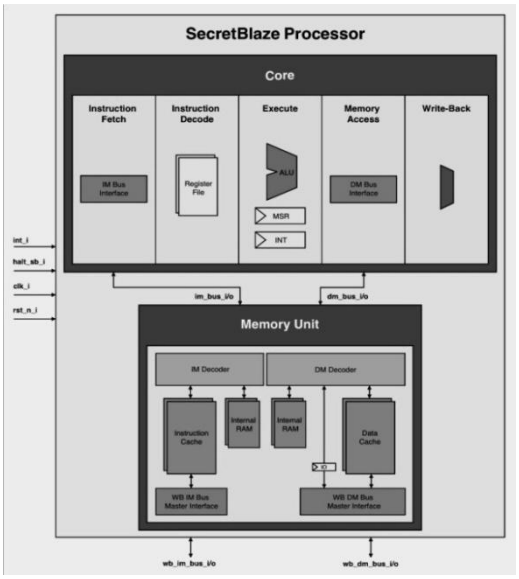

Fig. 6: The SecretBlaze Processor
[Source: www.lirmm.fr/ADAC].

This is the only processor with global hazard controller. The global hazard controller handles data and branch hazards by providing synchronous stall and flush signals for appropriate pipeline stages. It combines both, distributed and centralized control path methods. This approach balances the design quality and efficiency of Secret Blaze's data path. The data path supports several optional instructions to provide design flexibility to user. These instructions include barrel shifter operations, pattern comparators, integer multiplications and integer divisions. The performance of SecretBlaze is quite close to that of MicroBlaze [10].

G. LatticeMico32

The LatticeMico32 is an open-source 32-bit RISC Harvard architecture soft-core processor from Lattice Semiconductor and is shown in fig. 7.

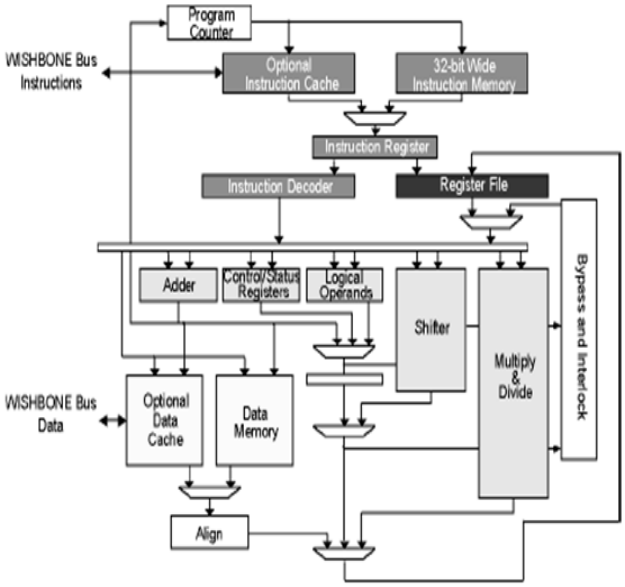

Fig. 7: LatticeMico32 Block Diagram [11].

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It combines a 32-bit wide instruction set with 32 general purpose registers, giving performance and flexibility to LatticeMico32, suitable for a wide variety of applications. It can handle up to 32 external interrupts and supports optional instruction and data caches. The core consumes minimal device resources, while maintaining the performance required for a broad application set. It doesn't have a floating-point unit. Instruction pipeline for this processor is 6-stage deep.

To speed up the development of microprocessor systems, several optional Wishbone compatible peripheral components may be integrated with the LatticeMico32 [11].

H. LEON3

The LEON3 is a 32-bit processor based on the SPARC V8 architecture and is designed and maintained by Aeroflex Gaisler AB in Sweden. The model is highly configurable and particularly suitable for system-on-a-chip (SOC) designs. The structure of LEON3 processor is shown in fig. 8. It follows Harvard architecture and uses the AMBA Advanced High-performance Bus (AHB) for all on-chip communications. Its main features include a 7-stage pipeline, separate instruction and data caches, configurable number of register windows within the limit of the SPARC standard and an optional floating-point unit. Register windowing makes it possible to select a new set of local registers upon a procedure, thereby reducing time required for storing register contents in memory every time. By default a basic implementation has 8 global registers, 8 sets of register windows, and each window consisting of 24 registers.

Thus at any time, 32 registers will be available for a program, out of the existing 200 registers [12]. The unique debug interface of LEON3 allows non- intrusive hardware debugging and provides access to all registers and memory. A main advantage of LEON3 processor is that it uses a structured organization of packets, folders and VHDL records. This processor is very reliable and hence is used in a large number of military and space applications [2]. Complete source code of this processor is available for free and unlimited use in research and education activities, under the GNU GPL license.

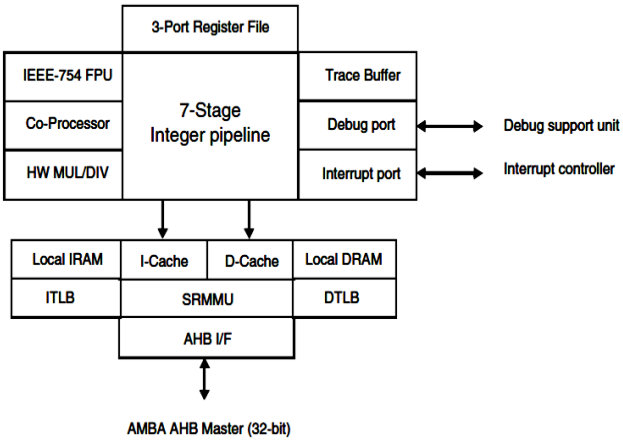

Fig. 8: Structure of LEON3 Processor [12].

Linux and RTOS can be installed on this processor. Not all FPGA development boards are supported by LEON3 [3].

I. OpenFire 0.3b

This 32-bit RISC processor is considered as a clone of Xilinx MicroBlaze soft-core processor and it executes a subset of the MicroBlaze instruction set. It doesn't have those instructions and functionality which are not needed in a processor array. The main features of this core include 32-bit instruction and data words, support for all basic arithmetic operations and a 3-stage instruction pipeline. The speed and performance of OpenFire is exactly same as that of the MicroBlaze for every implemented instruction with only an exception of the hardware multiplier on the OpenFire, which introduces five cycles of latency while the same in MicroBlaze has three cycles. Performance of the OpenFire is comparable to the MicroBlaze in Dhrystone MIPS and area. The comparison between OpenFire and minimal MicroBlaze implementation (no OPB, cache, and barrel shifter or hardware divider) shows that the OpenFire is 13% smaller and less than 1% slower in version 2.1 of the Dhrystone benchmark. The reason for slight difference in DMIPS is mostly the OpenFire's longer multiply latency [3].

J. aeMB

The aeMB is an implementation of soft-ware compatible MicroBlaze core. The compatibility is at cycle and instruction levels only and not at architecture levels. aeMB has Harvard architecture with separate 32-bit instruction and data buses. It uses the Wishbone interface for both data and instruction memory bus and supports configurable address space for each bus. Its CPU core is capable of moving and manipulating data to and from memory. The CPU has no peripherals or interrupt controllers, but supports external interrupts. One can map any peripherals and their respective registers to the data memory space. A short 3-stage integer pipeline, capable of executing one instruction per clock, allows fast context switching. It supports hardware multiplier and barrel shifter [3].

K. Tensilica's Xtensa

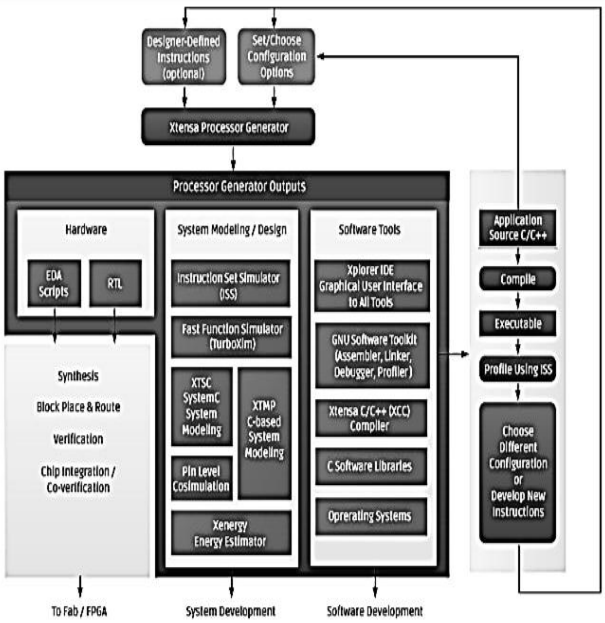

Fig. 9: The Xtensa Architecture [13].

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This is the flagship product of Tensilica. The Xtensa is a series of configurable and extensible processors. It's detailed architecture is shown in fig. 9. The main architectural features include Hardware multipliers, single precision IEEE-754 compatible FPU, varying number of interrupts, cache sizes and write policies, variable instruction and data memory sizes etc. The Tensilica Instruction Extension (TIE) language, allows designers to invent custom instructions. The TIE instructions are turned into hardware using the TIE compiler. The Xtensa Xplorer is complete design environment for Xtensa processors [13].

L. Cortex – M1:

This is a proprietary 32-bit processor using ARMv6 architecture and for using this processor, we need to get a license from ARM limited. Its features are described in fig. 10. The main features of Cortex-M1 include a 3-stage pipeline, configurable instruction and data memories (upto 1 MB), integrated interrupt controller with support upto 32 interrupts and has AMBA AHB-Lite 32-bit bus interface. It implements high density Thumb-2 instruction set.

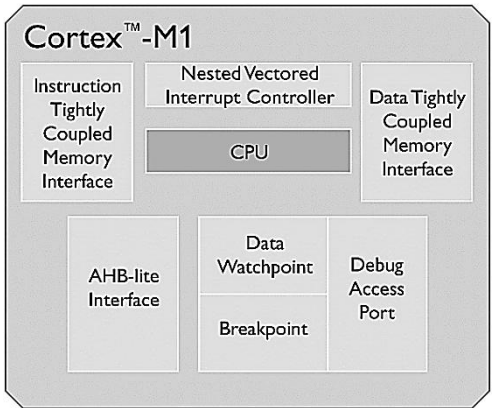

Fig. 10: Cortex – M1 Processor [14].

Cortex-M1 processor can deliver 0.8 DMIPS/MHz. It can be used with any FPGA [14].

M. eSi RISC

eSi-RISC is the only architecture licensed as an IP core that has both 16 and 32-bit implementations.

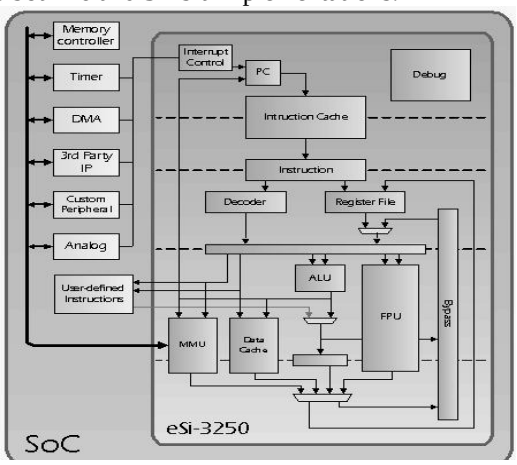

Fig. 11: eSi RISC Processor [15].

16 and 32-bit instructions in the eSi-RISC architecture can be freely intermixed resulting in improved code density without compromising performance. It has a Configurable 16 or 32-bit data-path. The details about the same are shown in fig. 11. It can handle up to 32 external interrupts and supports integer, floating-point and fixed-point arithmetic. It also provides optional support for user-defined instructions, such as cryptographic acceleration. Caches are also configurable and optional in terms of size and associativity [15] [16]. Available bus interfaces are AMBA AXI, AHB and APB. It has a 5-stage pipeline and hardware JTAG debugger.

N. ARC HS36 CPU

This is a 32-bit processor capable of delivering up to 3100 DMIPS and 5580 CoreMark at 1.61 GHz on 28HPM (worst case conditions). It is based on advanced ARCv2 ISA and supports a high degree of configurability, custom instructions and close coupling of memory and direct-mapped peripherals.

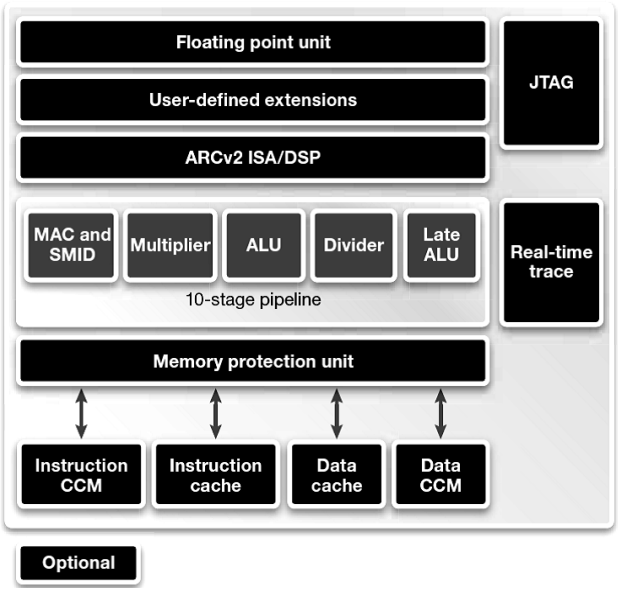

Fig. 12: ARC HS36 Processor Block Diagram [17].

ARC HS 36 has a high-speed, 10-stage pipeline with instruction and data cache ranging from 4KB to 64KB and it is available in dual-core and quad-core versions for higher performance.

As shown in fig. 12, its1MB instruction and data close coupled memory (CCM) and support to up to 240 interrupts makes it suitable for applications where high performance is required. Available bus interfaces are AMBA AXI, AHB ARM. It also provides JTAG and Compact JTAG (cJTAG) debug interface [17].

O. DSPuva 16

The **DSPuva16** has been developed at the Department of Electronics Technology of the University of Valladolid (Spain). It is basically a Digital Signal Processor and has a RISC architecture based on two 24-bit buses and handles 16/24 bits data. The main feature of DSPuva16 is it has a dedicated hardware multiplier-accumulator (MAC). It has 16 internal 24-bit registers, it allows to execute programs up to 256~4K instructions. Its instruction set is limited to 40 different instructions, and all of them are executed in one instruction cycle (including multiplications). Though it occupies very small area, it has very small program memory and no data memory [21].

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P. Few Other Soft Core Processors

Apart from the soft core processors discussed, a variety of soft cores are available from different manufacturers. The popular ones are like PicoBlaze, LatticeMico8. These are 8-bit RISC architectures developed by Xilinx and Lattice Semiconductors respectively. PicoBlaze is proprietary architecture but is tied to Xilinx devices only while LatticeMico8 is an open source architecture written in device independent HDL. An open-source clone of PicoBlaze i.e. PacoBlaze is also available with almost same features. It is a device independent CPU and is binary compatible with the PicoBlaze.

IV. CONCLUSION

In this paper, inspection of open-source as well as proprietary soft-core processors is done. **Table 1** shows comparison of major soft CPU's based on features like clock frequency, instruction pipeline stages, word length etc. In many applications one can use both a microprocessor and an FPGA array. There could be separate RISC CPU and FPGA chips. But these two entities can be combined in one chip, giving advantages like more flexibility in design, less power consumption, simpler board layout and fewer problems with signal integrity and EMI.

Table 1: Comparison of different soft core processors

Parameter / Soft Core Processor	Developing Organization	Open Source/ Proprietary	Word Length	Interface Bus standard	Clock Frequency	Pipeline Stages
OpenSPARC T1	Sun Microsystems	Open Source	64-Bits	JBI, SSI	200 MHz	6-stages
RISC S1	Sun Microsystems	Open Source	64-Bits	Wishbone, AMBA	--	6-stages
Open RISC 1200	Open Cores	Open Source	32-Bits	Wishbone	300 MHz	5-stages
Nios II	Altera	Proprietary	32-Bits	Avalon	200 MHz	6-stages
MicroBlaze	Xilinx	Proprietary	32-Bits	AXI, DPB, LMB	200 MHz	3-stages
SecretBlaze	LIRMM, CNRS	Open Source	32-Bits	Wishbone	90.0 MHz	5-stages
Lattice Mico 32	Lattice Semi.	Open Source	32-Bits	Wishbone	85–115 MHz	6-stages
LEON3	Aeroflex Gaisler	Open Source	32-Bits	AMBA2	400 MHz	7-stages
OpenFire 0.3b	Virginia Tech CCM Lab	Open Source	32-Bits	OPB, FSL	198 MHz	3-stages
aeMB	Shawn Tan	Open Source	32-Bits	Wishbone	279 MHz	3-stages
Xtensa	Tensilica	Proprietary	32-Bits	PIF, XLMI	350 MHz	5-stages
Cortex M1	ARM	Proprietary	32-Bits	AMBA AHB Lite	--	3-stages
eSi RISC	EnSilica	Proprietary	16/32-Bits	AMBA, AXI, AHB, APB	--	5-stages
ARC HS 36	ARC International	Proprietary	32-Bits	AMBA, AXI, AHB	1.61 GHz	10-stages
DSPuva16	University of Valladolid	Open Source	16/24-Bits	--	--	--

Soft-core processors are normally used for creating an FPGA based SoC. By virtue of this technology, we can reduce time periods of processor creation life cycle with the help of recently available EDA tools.

The embedded world is looking forward for more sophisticated reconfigurable devices with features like least power consumption, highest level of adaptability, small size, capability of run-time reconfiguration and ability to work with adaptive hardware algorithms.

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BIOGRAPHIES

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